Please replace the paragraph beginning at page 3, line 17, with the following replacement paragraph:

--In each unit pixel of the solid-state image pickup device thus constructed, there are a selection switch and a read-out switch. Accordingly, the pixel signal can be read out for every pixel. Therefore, the vertical signal line is first reset, and then each pixel signal is read out to the vertical signal line, whereby the reset level and the signal level are obtained in this order pixel by pixel. Further, by calculating the difference between the reset level and the signal level, the noise component due to the dispersion of the pixel characteristic can be cancelled. In addition, the reset level and the signal level are output through the same route, so that any stripe-shaped noise component having correlation in the vertical direction does not occur in principle.--

A2

Please replace the paragraph beginning at page 13, line 17, with the following replacement paragraph:

--As described above, the neighboring portions of the gate electrodes 13a, 14a of the selection MOS transistor 13 and the read-out MOS transistor 14 are overlapped with each other, whereby the n^+ diffusion region shown in Fig. 4 does not occur between the gate electrodes 13a, 14a, so that the noise component due to the dispersion of the field occurring in the gate electrode 14a of the read-out MOS transistor 14 at the shift timing from the period d to the period e can be also completely transferred.--

A3

Please replace the paragraph beginning at page 15, line 11, with the following replacement paragraph:

--Further, a vertical scan circuit 63 for line selection and a horizontal scan circuit 64 for column selection are provided. Each of these scan circuits 63 and 64 comprises a shift register, for example. The vertical scan pulse ΦVm output from the vertical scan circuit 63 is applied to the vertical selection line 56, the read-out pulse ΦCn output from the horizontal scan circuit 64 is applied to the read-out pulse line 57, a horizontal scan pulse ΦHn is applied to the gate electrode of the horizontal selection MOS transistor 60, and a reset pulse ΦRn is applied to the gate electrode of the reset MOS transistor 62. A CDS circuit 66 having the circuit construction shown in Fig. 5 is provided as a differential circuit through a horizontal output amplifier 65.--

A4